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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,076	10/10/2003	Vivek Nautiyal	64476-00002USPX	3058

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Andre M. Szuwalski
Jenkens & Gilchrist, P.C.
Suite 3200
1445 Ross Ave.
Dallas, TX 75201-2799

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,076	NAUTIYAL ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,15 and 16* is/are rejected.

7)☒ Claim(s) *7-14 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: transistor "M213" in Figure 2. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in IDIA on 10/16/02. It is noted, however, that applicant has not filed a certified copy of the 1039/DEL/2002 application as required by 35 U.S.C. 119(b).

Specification

4. The disclosure is objected to because of the following informalities: the specification fails to describe transistor M213 of Figure 2. Appropriate correction is required.

Claim Objections

5. Claim 1-20 are objected to because of the following informalities:

Claim 1, line 12, it appears that "inputs a cross-connected" should be changed to --input are cross-connected--.

Claims 2-6 are objected to because they include the informalities of claim 1.

Claim 5, line 2, "output node of the latch" should be changed to --output node of the output nodes of the latch--.

Claim 5, line 3-4, "output node of the latch" should be changed to --output node of the output nodes of the latch--.

Claim 7, line 2, "a first and second" should be changed to --a first output and a second--.

Claims 8-14 are objected to because they include the informalities of claim 7.

Claim 9, line 3, "a first latch inverter;" should be changed to --a first latch inverter of the cross-coupled latch inverters;--.

Claim 9, line 3, "a second latch inverter." should be changed to --a second latch inverter of the cross-coupled latch inverters.--.

Claim 12, line 3, "a first latch inverter;" should be changed to --a first latch inverter of the cross-coupled latch inverters;--.

Claim 12, line 3, "a second latch inverter." should be changed to --a second latch inverter of the cross-coupled latch inverters.--.

Claim 15, line 3, "first and second" should be changed to --first output and a second--.

Claims 16-20 are objected to because they include the informalities of claim 15.

Appropriate correction and/or clarification to the above matters are required so that the claims are clear.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitations "an enabling/disabling circuit connected between a supply terminal and a common conducting terminal of the latch" (line 4-5) and "whose conducting terminals are connected to the common conducting terminal of the latch" (line 12-13) are misdescriptive, and thus the claim is indefinite. As it is clearly describe in the specification and shown in the drawings, the enabling/disabling circuit (transistor M25) only connected to the common conducting terminal of transistors M210-M211 (which is the common conducting terminal of the set of inverters), and transistor M25 does not connected to a common terminal of the latch circuit (M21-M24). It is suggested that the recitation " and whose conducting terminals are connected to the common conducting terminal of the latch" (line 12-13) be changed to --an enabling/disabling circuit connected between a supply terminal and a common conducting terminal of the set of inverters--, and the recitation "an enabling/disabling circuit connected between a supply terminal and a common conducting terminal of the latch" (line 4-5) be deleted. Appropriate correction and/or clarification is requested.

Claims 2-6 are indefinite because they include the indefinite problem of claim 1.

Also in claim 4, "the first and second equalizing circuits are each a pair of MOS transistors with their control terminals tied together" is misdescriptive. Note the specification discloses that the first equalizing circuit includes only transistor M212, and the drawings shows that each of the first and second equalizing circuits includes only one transistor (i.e., transistor M212 for the first equalizing circuit and transistor M213 for the second equalizing circuit in Figure 2). Thus, the specification and the drawings do not disclose that each circuit includes a pair of MOS transistors as recited in claim 4. Appropriate correction and/or clarification is requested.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 15 rejected under 35 U.S.C. 102(b) as being anticipated by Kawasumi (US 2002/0024851 A1).

With respect to claim 15, Figure 7 of the Kawasumi reference discloses a sense amplifier circuit, which includes: a latch circuit (Q1-Q4) includes of cross-coupled first (Q1, Q3) and second (Q2, Q4) latch inverters and having a first output (drains of Q1 and Q3) and a second output (drains of Q2 and Q4); a first inverter (Q62, Q64) having an input coupled to the second output of the latch circuit (connected to the drains of Q2 and Q4 by way of the left-side transmission gate 3) and an output (drains of Q62 and Q64) connected to a first conducting line of the first latch inverter (the line connecting from the drains of Q1 and Q3 to the drains of Q62

and Q64 by way of the right-side transmission gate 3); and a second inverter (Q61, Q63) having an input coupled to the first output of the latch circuit (coupled to the drains of Q1 and Q3 by way of the right-side transmission gate 3) and an output coupled to a second conducting line of the second latch inverter (the line connecting from the drains of Q2 and Q4 to the drains of Q61 and Q63 by way of the left-side transmission gate 3).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasumi (US 2002/0024851 A1) in view of Jung et al. (USP 5,796,273).

With respect to claim 16, the circuit in Figure 7 discloses the sense amplifier circuit which includes a first equalizing circuit (Q8) and all of the limitations of this claim as discussed above (see the 102 rejection of claim 15) except for a second equalizing circuit coupled between the outputs of inverters (Q61-Q64). However, the Jung et al. reference discloses the advantage of having an equalizing circuit (Q9, Figure 2) coupled between the outputs of sense-amplifier is for increasing the speed of the sensing (Col. 5, lines 44-56). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 7 of the Kawasumi reference to provide an equalizing circuit (Q9, Figure 2 of Jung et al.) connected between the outputs of inverters (Q61-Q64, Figure 7 of Kawasumi) for the purpose of increasing the sensing speed of the circuitry. Thus, this modification meets all the limitations of

claim 16 as the modification's circuitry now including a second equalizing circuit (Q9, Figure 2 of Jung et al.) coupled between the first and second conducting lines.

Allowable Subject Matter

12. Claims 1-6 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claim 1, if amended as suggested above, would be allowed because the prior art of record fails to disclose or suggest the sense amplifier includes, in combination wither other limitations, the feedback means, the access control transistors and the set of inverters with the recited connections and operations set forth therein.

Claims 2-6 would be allowed because they depend on claim 1.

13. Claims 7-14 would be allowed if amended to overcome the minor informalities above.

Claim 7 would be allowed because the prior art of record fails to disclose or suggest the sense amplifier includes, in combination wither other limitations, a feedback circuit, a first access transistor and a second access transistor with the recited connections and operations set forth therein.

Claims 8-14 would be allowed because they depend on claim 7.

14. Claims 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the informalities set forth above.

Claim 17 would be allowed for the similar reason as indicated in claim 7.

Claims 18-20 would be allowed because they depend on claim 17.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 25, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816